Probabilistic Computing on FPGA with NIOS II soft-processor

Summary: The aggressive scale down in process technology, to increase its performance and reduce its power, has led to nano-devices with increased variation and limited resilience, exhibiting a stochastic behavior, inspired by biochemical cell signaling. We plan to take advantage of the uncertainty exhibited by new devices, and emulate its behavior on an FPGA.

Moreover, we plan to create a stochastic accelerator, using Bayesian gates, and integrate it in an embedded system as means to improve the efficiency of a DSP application (performance / power). Bayesian gates operate on probability distributions on binary variables as the building blocks of our probabilistic algebra. These Bayesian gates can be seen as a generalization of logical operators in Boolean algebra.

In this research project you will investigate the implementation of probabilistic computation accelerator as part of an embedded system using Altera’s soft-processor NIOS II.

Work Plan: The following tasks are planned for this topic: T1 requirement assessment, decision on the approach and training in implementing and debugging embedded systems using Qsys/Modelsim; T2 design the stochastic accelerator; T3 integration of the stochastic accelerator in the embedded system; T4 experimental validation of the solution; T5 writing the final dissertation. The end result is a dissertation and an implementation of the stochastic accelerator for NIOS II.

Supervisor: Prof. Jorge Lobo (DEEC-FCTUC), co-supervisor: Dr. Rui Duarte (ISR Coimbra)

This work is within the scope of the BAMBI European FET Project (FET Project - FP7-ICT-2013-C). The project takes a bottom-up approaches to building machines dedicated to Bayesian inference. Within the BAMBI consortium, ISR-UC is working on the emulation hardware implementation and on the computational architecture to be developed, namely in the composition of basic building blocks for probabilistic computation. http://mrl.isr.uc.pt/projects/bambi/

References:

The work will be carried out at the Institute of Systems and Robotics, ISR, in a lab fully equipped for FPGA prototyping and artificial perception. For more details, please contact jlobo@isr.uc.pt and visit http://ap.isr.uc.pt.
Probabilistic Computing on FPGA using OpenCL

Summary: The aggressive scale down in process technology, to increase its performance and reduce its power, has led to nano-devices with increased variation and limited resilience, exhibiting a stochastic behavior, inspired by biochemical cell signaling. We plan to take advantage of the uncertainty exhibited by new devices, and emulate its behavior on an FPGA.

Moreover, we plan to create a stochastic accelerator, using Bayesian gates, and integrate it in an embedded system as means to improve the efficiency of a DSP application (performance / power). Bayesian gates operate on probability distributions on binary variables as the building blocks of our probabilistic algebra. These Bayesian gates can be seen as a generalization of logical operators in Boolean algebra.

Recently, OpenCL has emerged as a framework to create, emulate and implement designs on FPGAs, opposed to traditional RTL design.

In this research project you will investigate the design of a stochastic accelerator using OpenCL, and integrate it on a computational system as means to improve the performance of computational intensive algorithms over traditional deterministic implementations.

Work Plan: The following tasks are planned for this topic: T1 requirement assessment, decision on the approach and familiarization with the OpenCL tool flow; T2 design of the stochastic accelerator; T3 integration of the stochastic accelerator in the computational system; T4 experimental validation of solution; T5 writing the final dissertation. The end result is a dissertation and an implementation of the stochastic accelerator using OpenCL.

Supervisor: Prof. Jorge Lobo (DEEC-FCTUC), co-supervisor: Dr. Rui Duarte (ISR Coimbra)

This work is within the scope of the BAMBI European FET Project (FET Project - FP7-ICT-2013-C). The project takes a bottom-up approaches to building machines dedicated to Bayesian inference. Within the BAMBI consortium, ISR-UC is working on the emulation hardware implementation and on the computational architecture to be developed, namely in the composition of basic building blocks for probabilistic computation. http://mrl.isr.uc.pt/projects/bambi/

References:

The work will be carried out at the Institute of Systems and Robotics, ISR, in a lab fully equipped for FPGA prototyping and artificial perception. For more details, please contact jlobo@isr.uc.pt and visit http://ap.isr.uc.pt
Probabilistic Computing on FPGA with OpenRISC

Summary: The aggressive scale down in process technology, to increase its performance and reduce its power, has led to nano-devices with increased variation and limited resilience, exhibiting a stochastic behavior, inspired by biochemical cell signaling. We plan to take advantage of the uncertainty exhibited by new devices, and emulate its behavior on an FPGA.

Moreover, we plan to create a stochastic accelerator, using Bayesian gates, and integrate it in an embedded system as means to improve the efficiency of a DSP application (performance / power). Bayesian gates operate on probability distributions on binary variables as the building blocks of our probabilistic algebra. These Bayesian gates can be seen as a generalization of logical operators in Boolean algebra.

In this research project you will investigate the implementation of probabilistic computation accelerator as part of an embedded system using OpenCore's soft-processor OpenRISC 1000 (OR1k).

Work Plan: The following tasks are planned for this topic: T1 requirement assessment, decision on the approach and familiarization with the OpenRISC tool flow; T2 design the stochastic accelerator; T3 integration of the stochastic accelerator in the embedded system; T4 experimental validation of the solution; T5 writing the final dissertation. The end result is a dissertation and an implementation of the stochastic accelerator for the OpenRISC soft-processor.

Supervisor: Prof. Jorge Lobo (DEEC-FCTUC), co-supervisor: Dr. Rui Duarte (ISR Coimbra)

This work is within the scope of the BAMBI European FET Project (FET Project - FP7-ICT-2013-C). The project takes a bottom-up approaches to building machines dedicated to Bayesian inference. Within the BAMBI consortium, ISR-UC is working on the emulation hardware implementation and on the computational architecture to be developed, namely in the composition of basic building blocks for probabilistic computation. [http://mrl.isr.uc.pt/projects/bambi/](http://mrl.isr.uc.pt/projects/bambi/)

References:
- OpenRISC - [http://opencores.org/or1k/Main_Page](http://opencores.org/or1k/Main_Page)

The work will be carried out at the Institute of Systems and Robotics, ISR, in a lab fully equipped for FPGA prototyping and artificial perception. For more details, please contact jlobo@isr.uc.pt and visit [http://ap.isr.uc.pt](http://ap.isr.uc.pt).
Probabilistic Computing on FPGA using Stochastic Arithmetic

**Summary:** The aggressive scale down in process technology, to increase its performance and reduce its power, has led to nanodevices with increased variation and limited resilience, exhibiting a stochastic behavior, inspired by biochemical cell signaling. We plan to take advantage of the uncertainty exhibited by new devices, and emulate its behavior on an FPGA.

Moreover, we plan to create a stochastic accelerator, using Bayesian gates, and integrate it in an embedded system as means to improve the efficiency of a DSP application (performance / power). Bayesian gates operate on probability distributions on binary variables as the building blocks of our probabilistic algebra. These Bayesian gates can be seen as a generalization of logical operators in Boolean algebra.

In this research project you will investigate the design and implementation of computational units based on the Bayesian gates on an FPGA.

**Work Plan:** The following tasks are planned for this topic: T1 requirement assessment, decision on approach and training in implementing and debugging embedded system using Quartus/Modelsim; T2 design of the stochastic accelerator; T3 integration of the stochastic accelerator in the embedded system; T4 experimental validation of solution; T5 writing of final dissertation. The end result is a dissertation and an implementation of the stochastic accelerator with NIOS II or in a stand alone stream processor.

**Supervisor:** Prof. Jorge Lobo (DEEC-FCTUC), co-supervisor: Dr. Rui Duarte (ISR Coimbra)

This work is within the scope or the BAMBI European FET Project (FET Project - FP7-ICT-2013-C). The project takes a bottom-up approaches to building machines dedicated to Bayesian inference. Within the BAMBI consortium, ISR-UC is working on the emulation hardware implementation and on the computational architecture to be developed, namely in the composition of basic building blocks for probabilistic computation. http://mrl.isr.uc.pt/projects/bambi/

**References:**

The work will be carried out at the Institute of Systems and Robotics, ISR, in a lab fully equipped for FPGA prototyping and artificial perception. For more details, please contact jlobo@isr.uc.pt and visit http://ap.isr.uc.pt.
Stereo-Inertial 3D Perception Embedded System for UAVs

Summary: In many environments where it is difficult, or dangerous, for someone to reach, it is important to have an autonomous system that can explore the environment.

Inertial-Visual sensors have been used in navigation systems, stereo image reconstruction, map generation and visual inspection. Moreover, not only Inertial-Visual (I-V) sensors can be used indoors, as they offer more accuracy than typical GPS systems, thus they can be used into a new series of applications that couldn’t be tackled before.

In this project you will explore the capabilities of the I-V sensor from Skybotix, a stereo-inertial sensing system with an embedded FPGA, to do a 3D reconstruction using data from a flying quadcopter.

Work Plan: The following tasks are planned for this topic: T1 requirement assessment, decision on approach and interface the Inertial-Visual sensor; T2 generation of the 3D reconstruction from the I-V sensor; T3 integration of the I-V sensor with the quadcopter; T4 experimental validation of solution; T5 writing of final dissertation. The end result is a dissertation and using the data of the I-V sensor as part of an autonomous system.

Supervisor: Prof. Jorge Lobo (DEEC-FCTUC), co-supervisor: Dr. Rui Duarte (ISR Coimbra)

This work is within the scope or the BAMBI European FET Project (FET Project - FP7-ICT-2013-C). The project takes a bottom-up approaches to building machines dedicated to Bayesian inference. Within the BAMBI consortium, ISR-UC is working on the emulation hardware implementation and on the computational architecture to be developed, namely in the composition of basic building blocks for probabilistic computation. http://mrl.isr.uc.pt/projects/bambi/

References:
- http://www.skybotix.com/

The work will be carried out at the Institute of Systems and Robotics, ISR, in a lab fully equipped for FPGA prototyping and artificial perception. For more details, please contact jlobo@isr.uc.pt and visit http://ap.isr.uc.pt.