

CURRICULUM VITÆ – OCTOBER 2025

GENERAL INFORMATION

NAME: Gabriel Falcão Paiva Fernandes
DATE OF BIRTH: 13.07.1974
NATIONALITY: Portuguese

HOME ADDRESS: Praça Cultural, N.21
3080-456 Figueira da Foz
Portugal

EMPLOYMENT: Associate Professor (with Tenure) at the Department of Electrical and Computer Engineering, FCTUC, University of Coimbra, Portugal

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ACADEMIC DEGREES

08/2006-12/2010 **PhD in Electrical and Computer Engineering** at the Faculty of Science and Technology of the University of Coimbra (FCTUC), in the area of Telecommunications and Microelectronics under the subject: "**Parallel Algorithms and Architectures for LDPC Decoding**";

06/2002 MSc in Electrical and Computer Engineering at the Faculty of Engineering of the University of Porto (FEUP), in the area of Digital Audio Signal Processing under the subject: "DSP Implementation of a Real-Time Analyzer System – Applied to Adaptive Equalization";

1992-1997 BSc (a 5 years degree) in Electrical and Computer Engineering at the Faculty of Engineering of the University of Porto (FEUP), in the area of Telecommunications;

1989-1992 Technical and Professional course of Electronics, at the "Colégio Internato dos Carvalhos", in Porto.

POSITIONS

08/2025-07/2026 **Visiting Associate Professor** at the Computer Science Department, New York University (**NYU**), Abu Dhabi, UAE;

07/2024 Associate Professor at the Department of Electrical and Computer Engineering, Faculty of Science and Technology of the University of Coimbra (FCTUC), Coimbra, Portugal;

07/2018-08/2018 **Visiting Academic** at the Computer Science Department, Eidgenössische Technische Hochschule Zürich (**ETHZ**), Zürich, Switzerland;

2017-2018	Visiting Professor at the School of Computer & Communication Sciences, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland;
02/2015	Tenured Assistant Professor at the Department of Electrical and Computer Engineering, FTUC, University of Coimbra, Coimbra, Portugal;
2011-2012	PostDoc at the School of Computer & Communication Sciences, EPFL , Lausanne, Switzerland;
2010-2015	Assistant Professor at the Department of Electrical and Computer Engineering, FCTUC, University of Coimbra, Coimbra, Portugal;
2007-2010	Invited researcher at <i>INESC-ID</i> , in the Signal Processing Systems (SiPS) group devoted to the research of algorithms and architectures for signal processing systems, Lisbon;
2004-present	Researcher at <i>Instituto de Telecomunicações</i> (a R&D institute), in the area of Microelectronics and Signal Processing, Coimbra;
2003-2010	Teaching Assistant at the Electrical and Computer Engineering Department, FCTUC, University of Coimbra, Coimbra, Portugal;
02/2000-06/2000	Lecturer in the support of laboratorial classes, teaching "Real-Time Signal Processing", one-semester course of the last year of the graduation studies on Electrical and Computer Engineering at the Faculty of Engineering of the University of Porto (FEUP), Porto;
10/1997-12/2002	Researcher (with scholarship) at the Telecommunications and Multimedia Unit, INESC Porto (now INESC TEC, a R&D institute), in the area of Digital Audio Signal Processing, Porto.

TEACHING

09/2018-present	<i>High-Performance Heterogeneous Computing</i> , one-semester course of the 2nd year of the master of science studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
09/2018-present	<i>Capstone Project I</i> , one-semester course of the 2nd year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
02/2013-07/2017	<i>Computer Architecture</i> , one-semester course of the 1st year of the graduation studies on Informatics Engineering / Computer Science, FCTUC, University of Coimbra;
02/2013-07/2017	<i>Microprocessor Systems</i> , one-semester course of the 1st year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
09/2007-02/2017	<i>Computer Technology</i> , one-semester course of the 1st year of the graduation studies on Informatics Engineering / Computer Science, FCTUC, University of Coimbra;
02/2003-07/2011	<i>Data Structures and Algorithms Programming in C/C++</i> , one-semester course of the 1st year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
09/2003-02/2007	<i>Project of Digital Systems</i> , one-semester course of the last year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
09/2003-02/2007	<i>Computer Programming in C/C++</i> , one-semester course of the 1st year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;

09/2003-02/2006	<i>Computer Programming in Python</i> , one-semester course of the 2th year of the graduation studies on Biomedical Engineering at the Department of Physics, FCTUC, University of Coimbra;
02/2003-07/2007	<i>Digital Electronics</i> , one-semester course of the 4th year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
02/2003-07/2003	<i>Microwave Communications</i> , one-semester course of the last year of the graduation studies on Electrical and Computer Engineering, FCTUC, University of Coimbra;
02/2000-07/2000	<i>Real-Time Signal Processing</i> (as TA), one-semester course of the last year of the graduation studies on Electrical and Computer Engineering at FEUP, Faculty of Engineering of the University of Porto.

MANAGEMENT AT THE UNIVERSITY

02/2020-01/2023	Coordinator of the doctoral programmes on Electrical and Computer Engineering, and Electrical Engineering and Intelligent Systems, FCTUC, University of Coimbra (100+ students);
10/2021-09/2023	Member of the Scientific Council in Electrical and Computer Engineering at the University of Coimbra (1st term);
10/2023-present	Member of the Scientific Council in Electrical and Computer Engineering at the University of Coimbra (2nd term);

PROFESSIONAL SERVICE

9/2024	Guest Editor of the Special Issue 'Past, Present and Future of Warehouse-Scale Computing' at IEEE Micro Magazine, September / October 2024 (led by Prof. John Hennessy , Stanford & Alphabet Inc.);
6/2023	Associate Editor of IEEE Transactions on Signal Processing ;
2/2023	Associate Editor of IEEE Micro (Magazine);
9/2022	Leading Guest Editor of the Special Issue ' AI at the Edge ' at IEEE Micro (Magazine), September 2022;
7/2022	Leading Guest Editor of the Special Issue 'Advances in Signal Processing Systems' at the Journal of Signal Processing Systems, Springer, July 2022;
2017 to 2024	Member of the Technical Program Committee of the IEEE International Conference on Audio, Speech and Signal Processing Systems (ICASSP);
2017 to 2024	Member of the Technical Program Committee of the IEEE International Workshop on Signal Processing Systems (SiPS);
2022 to 2024	Member of the International Program Committee of High-Performance Graphics (HPG);
2021 and 2022	Member of the Program Committee of IEEE/ACM International Conference on Computer-Aided Design (ICCAD);
9/2021	Local Chair of Euro-par 2021 , Lisbon, Portugal, 30 August-3 rd September 2021;

- 10/2020 and 2021 **Global Co-Chair of the IEEE International Workshop on Signal Processing Systems (SiPS)**, Coimbra, October 2020 (SiPS 2020) and October 2021 (SiPS 2021)—event repeated in virtual Coimbra due to the pandemics;
- 5/2017 Member of the Technical Program Committee of the 14th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), York, UK, 1-3rd July 2019 (ReCoSoC 2019);
- 4/2019 Member of the Technical Program Committee of the International Workshop HeteroPar'2019 (Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms), Göttingen, Germany, 26-30th August 2019;
- 4/2018 Member of the Program Committee of the International Conference on Biometric Engineering and Applications (ICBEA), Amsterdam, The Netherlands, 16-18th May 2018 (ICBEA 2018);
- 4/2017 Member of the Technical Program Committee of the 15th International Workshop HeteroPar'2017 (Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms), 28th August 2017;
- 3/2015 Member of the Technical Program Committee of the 18th CSI International Symposium on Computer Architecture & Digital Systems, 7-8 October 2015 (CADS 2015);
- 2/2014 Member of the Technical Program Committee of the 22nd European Signal Processing Conference, Lisbon, 1-5 September 2014 (EUSIPCO2014);
- 2013 to 2016 Member of the Program Committee of the Portuguese Meetings on Reconfigurable Systems (REC2013);
- 07/2011 Member of the Organizing Committee of the Workshop on GPU 2011 – Programming for Scientific Applications, sponsored by NVIDIA and the Univ. of Texas at Austin, USA;
- 11/2011 Member of the Program Committee of the First International Workshop on Challenges on Massively Parallel Processors (CMPP2011).

GRANTS AND AWARDS

- 11/2025 Gabriel Falcão, 1st place **J. Norberto Pires 2025 Innovation Award**, for "G-quAI: Predicting Gastrointestinal Cancer using Quantum AI";
- 10/2024 Gabriel Falcão, top 10 and finalist of the OQI SDG Use Cases, presented at the **GESDA Summit 2024**, for "Predicting Gastrointestinal Cancer using Quantum Machine Learning";
- 10/2022 Gabriel Falcão, **HiPEAC Paper Award** for "pLUTo: Enabling Massively Parallel Computation In DRAM via Lookup Tables", by João Dinis Ferreira, Gabriel Falcao, Juan Gómez-Luna, Mohammed Alser, Lois Orosa, Mohammad Sadrosadati, Jeremie S. Kim, Geraldo F. Oliveira, Taha Shahroodi, Anant Nori, and Onur Mutlu, presented at the IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Chicago, United States, October 2022;
- 11/2020 Cláudio Gomes, MSc student at DEI-FCTUC, supervised by João P. Fernandes and Gabriel Falcão with the theme "Portfolio Optimization in Financial Markets using Quantum Computing", received a scholarship from the **Calouste Gulbenkian Foundation** for "**New Talents in Quantum Technologies**" (€2,500);
- 10/2017 Gabriel Falcão, **HiPEAC Paper Award** for "SCRATCH: An End-to-End Application-Aware Soft-GPGPU Architecture and Trimming Tool", by P. Duarte, P. Tomas and G. Falcao, presented at the IEEE/ACM

- International Symposium on Microarchitecture (**MICRO**), Boston, United States, October 2017;
- 12/2015 ANACOM URSI 2015 National Award for "Diffractionless Propagation of Electron Waves in Graphene Superlattices" (€4 000);
- 09/2013 **Best Paper Award** for paper "Camera calibration and real-time image distortion correction in medical endoscopy using exchangeable optics", by Rui Melo, Joao Barreto, and Gabriel Falcao, 3rd Joint Workshop on New Technologies for Computer/Robot Assisted Surgery (CRAS), Verona, Italy, September 2013;
- 08/2013 **Google Faculty Research Award** for "UrbanScan: fast 3D modeling of urban scenes using a new stereo vision approach", (together with J. Barreto) project funded by Google Inc. (USD \$18 600);
- 07/2013 **1st place @ALTERA Europe-wide University Contest** 2012-2013, category of "Most commercially relevant use of an FPGA" for ON-OFF: Opencl-based NOn-binary ldpc decoding For FPGAs", by João Andrade, Gabriel Falcão, and Vítor Silva. The award was received at the International Conference on Field Programmable Logic and Applications (FPL), in September 2nd 2013;
- 05/2012 Gabriel Falcão, **HiPEAC Paper Award** for "Shortening design time through multiplatform simulations with a portable OpenCL golden-model: the LDPC decoder case", by Gabriel Falcao, M. Owaida, D. Novo, M. Purnaprajna, N. Bellas, C. D. Antonopoulos, G. Karakonstantis, A. Burg and Paolo Ienne, presented at the IEEE Symposium on **FCCM**, May 2012 (€1 000);
- 10/2010 Finalist and awarded with the **2nd** place at the **Fraunhofer Portugal Challenge**, in the category of PhD theses (€1 500);
- 12/2008 Grant by Fundação Jorge Álvares (€1 500);
- 10/2007-12/2010 Scholarship by Portuguese Foundation for Science and Technology (FCT) (€10 000);

RESEARCH GROUP AND RESEARCH TOPICS

- 2004- Computer architecture, Processing-in-memory, Microelectronics, VLSI Architectures (ASIC, FPGA), Quantum Computing, Parallel Computing (GPU, CPU, DSP), Parallel Programming, CUDA, OpenCL, HLS, VHDL, Verilog, Signal Processing, Low-Density Parity-Check (LDPC) codes, Deep learning, Medical Imaging and Medical Ultrasound Systems.

SPONSORED RESEARCH SUPPORTED BY THIRD-PARTY FUNDS (~1.6M€)

- 1/2025-5/2027 "G-quAI: Predicting Gastrointestinal Cancer Using Quantum AI, project developed at the University of Coimbra, funded by CERN and open Quantum Institute (OQI), Switzerland (**€70 000**);
- 3/2023-02/2026 "UNIFY: Compilation Abstraction and Hardware Adaptation for Specialized and General-Purpose Computing Unification", (Ref: 2022.06780.PTDC) project developed at INESC-ID/INESCTEC/IT-Coimbra / Universidade de Coimbra, funded by FCT (**€250 000**);
- 10/2021-05/2023 "Bin-NET: PiM-Enabled Binary Neural Network Inferencing at the Edge", (Ref: EXPL/EEI-HAC/1511/2021) project developed at IT-Coimbra / Universidade de Coimbra, funded by FCT (**€49 997**);
- 07/2018-06/2022 "HANdle: Hardware Accelerated Deep LEarning framework", (Ref: PTDC/EEI-HAC/30485/2017) project developed at INESC-ID/IST e IT-Coimbra/Universidade de Coimbra, funded by FCT / FEDER (**€239 997**);

04/2017-03/2018	"CRYPTOnITe", project developed at Instituto de Telecomunicações and University of Coimbra, funded by Instituto de Telecomunicações and FCT (€30 000);
08/2016-07/2018	"TopMater", project developed at Instituto de Telecomunicações and University of Coimbra, funded by Instituto de Telecomunicações and FCT (€60 000);
09/2013-09/2014	Google Research Award for "UrbanScan: fast 3D modeling of urban scenes using a new stereo vision approach", project developed at the University of Coimbra, and funded by Google (USD \$18 600);
01/2013-12/2015	"ASSISTED MOBILITY SUPPORTED BY SHARED-CONTROL AND ADVANCED HUMAN-MACHINE INTERFACES", project funded by the <i>COMPETE - Programa Operacional Factores de Competitividade e do Quadro de Referência Estratégica Nacional - QREN</i> (Ref: RECI/EEI-AUT/0181/2012), developed at the University of Coimbra, and funded (€437 558).
07/2013-06/2015	"Processamento de imagens e problemas inversos : aplicações em imagens médicas, imagens de observação terrestre, e em biomatemática", project funded by <i>Fundação para a Ciência e a Tecnologia</i> (Ref: PTDC/MAT-NAN/0593/2012), developed at the University of Coimbra, and funded (€113 830).
07/2006-09/2008	Tecnovoz - "Tecnologias de Reconhecimento e Síntese de Voz", project funded by the <i>Portuguese Ministry of Economy and Innovation, Program Prime</i> (Ref: PMDT Nº 03/165), developed at the Instituto de Telecomunicações, Pólo de Coimbra, URL: http://www.tecnovoz.pt and funded (€400 000).

MOST RELEVANT ACHIEVEMENTS

08/2013-2015	Google Faculty Research Award for "UrbanScan: fast 3D modeling of urban scenes using a new stereo vision approach", project funded by Google;
07/2013	João Andrade, Gabriel Falcão, and Vítor Silva, " ALTERA Europe-wide University Contest 2012-2013 ", category of " Most commercially relevant use of an FPGA " for ON-OFF: Opencl-based NOn-binary ldpc decoding For FPGAs", by João Andrade, Gabriel Falcão, and Vítor Silva. The award was received at the International Conference on Field Programmable Logic and Applications (FPL), in September 2 nd 2013;
01/2011	Book chapter published at the very prestigious and world famous book GPU Gems 3 series, Emerald Edition, Morgan kaufmann, ed. By Prof. Wen-mei Hwu (University of Illinois, USA);
10/2010	Finalist and awarded with the 2nd place at the Fraunhofer Portugal Challenge , in the category of PhD theses;
2008-2024	Select Papers: Communications of the ACM (2023), IF = 22.7 ; ACM Computing Surveys (2024), IF = 16.6 ; IEEE Communications Surveys & Tutoriasls (2021), IF = 35.6 ; IEEE Signal Processing Magazine (2012), IF = 9.4 ; IEEE/ACM International Symposium on Microarchitecture (MICRO'17 and '22), acceptance rate <18% ; IEEE International Conference on Computer Vision (ICCV'13), acceptance rate <20% ; Annual IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM'12 and '15), acceptance rate <22% ; 23 rd ACM International Conference on Supercomputing (ICS'09), acceptance rate <20% ; 13 th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP'08), acceptance rate <24% .

POST-DOCS SUPERVISION (COMPLETED)

- 07/2020-11/2021 Nuno Filipe Simões Santos Moraes Neves, "Hardware Accelerated Deep Learning Framework: Reconfigurable Machine-Learning Accelerators", Supervisor: G. Falcao (FCTUC);
- 04/2017-03/2018 Artur Miguel Mariano, "CRYPTOnITe: Testing the limits of parallel computer architectures under attacks against lattice-based cryptoschemes", Supervisor: G. Falcao (FCTUC);

SUPERVISION AND CO-SUPERVISION OF PH.D. STUDENTS (FIVE COMPLETED)

- 2025- Ana Fernandes, "Unlocking Sparse Processing with System-on-Chip Stream-based Acceleration", supervisors: Gabriel Falcao (FCTUC); Nuno Neves (INESC-ID/IST) [ECE] (ongoing);
- 2023- Hamid Moghadaspour, "Highly-Performant Underwater SLAM-Based 3D Reconstruction Architectures", supervisors: Gabriel Falcao (FCTUC); Nuno Neves (INESC-ID/IST) [ECE] (ongoing);
- 2023- Sofia Monteiro, Classifying functional impairments in Foot Clinic patients using plantar pressure distributions, supervisors: Joel Arrais (FCTUC); Gabriel Falcao (FCTUC) [PhD Programme in **Biomedical Engineering**] (ongoing);
- 2021- Cláudio Gomes, Quantum Computing for Sustainability, supervisors: J. Paulo Fernandes (FEUP); G. Falcao (FCTUC); Soumya Kar (CMU), Sridhar Tayur (CMU) [**Dual degree PhD in ECE @Portugal-CMU Doctoral Programme**] (ongoing);
- 2020-2025 Óscar Ferraz, Towards Processing Near-Memory in Non-Binary Low Density Parity Check Decoders, supervisors: G. Falcao (FCTUC); Vitor Silva (FCTUC) [ECE] (**completed**);
- 2020-2025 João Vieira, Enabling General-Purpose Processing-In-Memory Through a Locality-Aware Architecture and Compiler, supervisors: P. Tomás (IST); G. Falcao (FCTUC); Nuno Roma (IST) [PhD Programme in ECE at Instituto Superior Técnico] (**completed**);
- 2015-2020 João Gante, The Interplay Between Positioning and Beamforming in Millimeter Wave Communications [ECE] (**completed**);
- 2011-2016 João Andrade, Design space exploration of programmable and reconfigurables LDPC codes on multicore platforms [ECE] (**completed**);
- 2011-2015 Rui Melo, Camera calibration and real-time image processing in heterogeneous architectures [ECE] (**completed**).

SUPERVISION AND CO-SUPERVISION OF MSc. STUDENTS (ALL COMPLETED)

- 2024-2025 Daniel Faria, "Breast Cancer Detection in Ultrasound Imaging Using Weightless Neural Networks";
- 2024-2025 Joana Saraiva, "Polyp Detection using Weightless Neural Networks";
- 2023-2024 Diogo Gouveia, "A Parallel Computing Platform for Arthroscopic Video Synchronization in Augmented Reality Surgery Applications";
- 2023-2024 Afonso Carvalho, "Real-time AI Models Running on Low-power Embedded GPUs for Arthroscopic Surgery";
- 2023-2024 Joana Gonçalves, "Space Rider Maiden Flight Orbital Particles Identification using THOR Instrument and Machine Learning Techniques";

2022-2023	Ana Fernandes, "A Functional Validation Framework for the Unlimited Vector Extension";
2022-2023	Pedro Póvoa, "Combining HPC and low-power systems for data-intensive-acquisition sensors in space missions";
2021-2022	Bruno Simões, "Diabetic Retinopathy Diagnosis with Bag-of-Features and GPU-based Feature Extraction using SURF";
2021-2022	Diogo Correia, "GPU-Aided Optical Flow Tracking Application for Arthroscopy Surgery";
2021-2022	Adriano Durão, "Recurrent Neural Networks for Smiles Generation: Quantization Study";
2021-2022	Leonardo Galveias Esteves, "Federated Learning for IoT Edge Computing: An Experimental Study";
2020-2021	Cláudio Gomes, "Portfolio Optimization in Financial Markets using Quantum Computing: An Experimental Study";
2020-2021	Pedro Carrinho, "Exploiting Quantization in Convolutional Neural Networks for Polyp Detection on GPUs";
2020-2021	João Barreiros, "Fast Scale-Invariant Feature Transform on GPU";
2019-2020	António Fraga, "Parallel Face Detection";
2019-2020	Filipe Cabeleira, "On the Acceleration of Lattice Based Algorithms for Post-Quantum Cryptosystems";
2018-2019	Óscar Ferraz, "Combining Low-Power with Parallel Processing for Multispectral and Hypespectral Image Compression";
2017-2018	Alexandre Martins, "Compressor Multispectral e Hyperspectral Sem Perdas, Paralelo e de Baixo Consumo em GPU";
2017-2018	Eduardo Preto, "Framework para aquisição e processamentos rápido de imagens médicas do trato gastrointestinal em tempo real";
2017-2018	César Pereira, "Parallelization of monocular SLAM in real-time";
2017-2018	Pedro Barbosa, "CogniStim: Physical and cognitive real-time stimulator using inertial sensors in a virtual reality environment for elderly people";
2017-2018	Alexandre Martins, "A Low-power Parallel GPU Multispectral and Hyperspectral Lossless Compressor";
2017-2018	David Costa, "Treino Semiautomático de Sistemas de Reconhecimento de Fonemas baseado em Redes Neurais";
2015-2016	José Marques, "Distributed Learning of Convolutional Neural Networks on Heterogeneous Processing Units";
2015-2016	Guilherme Franco, "Phoneme recognition system for European Portuguese based on neural networks";
2015-2016	Pedro Duarte, "Application-specific Soft-GPGPU on Reconfigurable Substrates";
2014-2015	Manuel Rodrigues, "Electron wave propagation in graphene using parallel computing on GPUs with CUDA";
2014-2015	Ricardo Ralha, "Real-time symmetry-based dense stereo matching for 3D reconstruction";

2014-2015	Vasco Gama da Mota, "Efficient Implementation of Graph Cut Methods for Energy Minimization in Computer Vision Contexts";
2013-2014	Carlos Graça, "Acceleration of computer-assisted image inspection algorithms in medical scenarios";
2013-2014	Joao Maria, "Accelerating the Processing of Neural Networks for Object Recognition Using Low-power Devices";
2012-2013	João Amaro, "Synthetic aperture beamforming processing on GPUs using OpenCL";
2011-2012	Marco Martins, "Endoscopic Image Segmentation using Parallel Computing on GPUs with CUDA";
2009-2010	João Andrade, "DVB-S2 LDPC Decoder on GPUs";
2008-2009	João Cacheira, "Backend for DVB-S2 Parallel LDPC Decoder Architecture";
2007-2008	António Carvalho, "BCH+Interleaver+LDPC efficient hardware joint encoder for DVB-S2";
2007-2008	José Marinho, "Parallel LDPC decoder on a CELL Broadband Engine Architecture (PlayStation 3)";

SUPERVISION OF FINAL YEAR BSC GRADUATION PROJECTS

2006-2007	BCH coder and decoder for DVB-S2 Forward Error Control system implemented in Xilinx FPGAs*;
2005-2006	"Implementação da norma DVB-S2 em FPGA Xilinx – Modelos Verilog para Codificador/Descodificador LDPC e Interleaver/Deinterleaver" – LDPC coder and decoder with interleaver for the DVB-S2 Forward Error Control system implemented in Xilinx FPGAs*;
2004-2005	"Modelo Verilog para descodificadores LDPC – Aplicação à norma DVB-S2" – Hardware model (Verilog) of an LDPC decoder targeting the DVB-S2 standard*;
2003-2004	"audioDACdig Conversor Digital Analógico para Áudio" – Hardware model (Verilog) of the digital core of a Digital-to-Analog Audio Converter (DAC) based in oversampling and sigma-delta techniques*.

*Projects developed in partnership with Chipidea/MIPS Technologies Analog Business Group/Synopsys, where all students have currently a permanent position.

INVITED TALKS & PUBLIC PRESENTATIONS

6/2023	"Enabling Massively Parallel Computation in DRAM via Lookup Tables", Carnegie Mellon University (CMU), Pittsburgh, USA;
04/2022	"Quantum Computing: from Communications to Logistics", University of Coimbra;
11/2020	"Introduction to Arduino: From IoT to Medical Devices", Biomedical Engineering, University of Coimbra;
04/2019	"Application-specific soft-GPGPU for the LDPC decoder case", Amrita University, Bangalore, India;

07/2018	"PIM-Minded Multiplication", SAFARI / Systems Group, ETHZ, Switzerland;
11/2016	"Distributed Learning of Convolutional Neural Networks on Heterogeneous Processors", Computing Systems Week, Dublin, Ireland;
10/2016	"Accelerating the reconstruction of 3D urban scenarios", University of Porto, Porto, Portugal;
08/2016	"GPU-based accelerators for compute-intensive image and communications signal processing", Amrita University (virtual), India;
09/2015	"GPUs and parallel computing towards 3D reconstruction", Aalto University, Helsinki, Finland;
02/2014	"High performance computing", University of Coimbra, Portugal;
02/2013	"Heterogeneous parallel computing in surgical medical procedures: from theory to reality", University of Tsukuba, Japan;
05/2012	"GPU computing for speeding up highly demanding signal processing applications", University of Macao, China;
02/2012	"One single OpenCL kernel to program different multicores", Creative Electronic Systems (CES), Genève, Switzerland.

REVIEWING ACTIVITIES

- IEEE MICRO, 2024, 2023, 2022, 2013, 2023.
- IEEE Computer, 2021.
- Journal of Microprocessors and Microsystems, 2019, 2017.
- Journal of Real-Time Image Processing, 2020, 2019, 2017 e 2015.
- Journal of Parallel and Distributed Computing, Elsevier, 2014, 2013, 2011 e 2010.
- Parallel Computing, Elsevier, 2009.
- IEEE Computer Architecture Letters, 2012.
- IEEE Transactions on Parallel and Distributed Systems, 2023, 2019, 2017, 2015, 2014, 2013,
- IEEE Transactions on Computers, 2015, 2009.
- Journal of Systems Architecture, 2016
- Journal of Computer Science and Technology, 2021
- Concurrency and Computation: Practice and Experience, Journal, John Wiley and Sons, 2013.
- IEEE Transactions on Signal Processing, 2024, 2023.
- IEEE Journal of Biomedical and Health Informatics, 2022.
- IEEE Transactions on Medical Imaging, 2011.
- IEEE Transactions on Dependable and Secure Computing, 2020
- Journal of Signal Processing Systems, Springer, 2022, 2010.
- IEEE Access, 2020, 2024.
- IEEE Transactions on Circuits and Systems for Video Technology, 2015, 2014 e 2012.
- Neural Processing Letters, Springer, 2014.
- ACM Transactions on Embedded Computing Systems, 2016 e 2015.
- IEEE Communications Letters, 2013.
- Digital Signal Processing, Elsevier, 2012.
- IEEE Transactions on Multimedia, 2011.

INTELLECTUAL PROPERTY (PUBLISHED PATENTS LICENSED TO INDUSTRY: SMITH & NEPHEW)

07/2011	METHOD AND APPARATUS FOR AUTOMATIC CAMERA CALIBRATION USING ONE OR MORE IMAGES OF A CHECKERBOARD PATTERN. Pub. No. WO/2013/015699, International Application No.: PCT/PT2012/000030, Publication Date: 31.01.2013, International Filing Date: 25.07.2012, IPC: G06T 7/00 (2006.01), G01B 21/04 (2006.01), H04N 17/00 (2006.01), A61B 1/00 (2006.01). Inventors: Rui Melo, João P. Barreto, Gabriel Falcão.
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PROTOTYPES IMPLEMENTED FOR INDUSTRY

1997-1999	20 Band Digital Audio Equalizer based on a TMS320C31 DSP;
1998-2000	Real-Time Audio Decoder (ASCDEC: an INESC Porto's audio coding proprietary format) based on a TMS320C31 DSP;
2000-2001	3 Way Digital Crossover System based on an ADSP21065 SHARC DSP;
2000-2001	Sound Level Meter based on a TMS320VC5402 DSP;
2001-2002	Automatic Room Acoustics Correction System based on an ADSP21065 SHARC DSP.

BOOK CHAPTERS

[2022]

A. Mariano, F. Cabeleira, L. P. Santos, and G. Falcao. "Optimized Voronoi-based Algorithms for Parallel Shortest Vector Computation", Chapter in Kuan-Ching Li, Nitin Sukhija, Elizabeth Bautista, Jean-Luc Gaudiot, eds., *Cybersecurity & High-Performance Computing Environments: Integrated Innovations, Practices, and Applications*, CRC PRESS, Taylor & Francis, Florida, USA, Feb 2022.

[2015]

S. Yamagiwa, G. Falcao, K. Wada, and L. Sousa. "Stream-based Parallel Computing Methodology and Development Environment for High Performance Manycore Accelerators", Chapter in Thomas S. Clary, ed., *Horizons in Computer Science Research*, Volume II, Nova Science Publishers Inc., New York, USA, July 2015.

[2014]

S. Kumar, I. N. Figueiredo, C. Graca, and G. Falcao "A GPU Accelerated Algorithm for Blood Detection in Wireless Capsule Endoscopy Images", (accepted) Chapter in Tavares, J.M., Renato, R.S.N.J., eds. *Developments in Medical Image Processing and Computational Vision*, Lecture Notes in Computational Vision and Biomechanics, Springer, 2014.

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FOREIGN LANGUAGES

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French – spoken and written;
Spanish – spoken;

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